

Application No. 10/066,019

3

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 1. (currently amended) A crosspoint switch integrated circuit comprising:
2 an array of input ports;
3 an array of output ports;
4 a switch matrix configured to selectively connect said input ports
5 to said output ports for conducting electrical signals therebetween; and
6 equalization circuitry coupled to at least partially offset trans-
7 mission losses experienced by said electrical signal while external to said
8 crosspoint switch integrated circuit, said equalization circuitry being
9 configured to measure jitter within said electrical signals and to utilize jitter
10 measurements as a basis for offsetting said transmission losses, said
11 equalization circuitry being responsive to said jitter measurements to
12 automatically select levels of equalization.

1 2. (cancelled)

1 3. (original) The crosspoint switch integrated circuit of claim 1 wherein said
2 equalization circuitry includes a plurality of adjustable equalizers, said
3 adjustable equalizers each having adjustable filtering characteristics within a
4 fixed number of equalization settings.

1 4. (original) The crosspoint switch integrated circuit of claim 3 wherein each
2 said adjustable equalizer includes a plurality of switchable connections which
3 individually adjust said filtering characteristics when activated.

Application No. 10/066,019

4

1 5. (original) The crosspoint switch integrated circuit of claim 4 wherein each
2 said switchable connection includes a switch, at least some of said switchable
3 connections including at least one component which significantly affects said
4 filtering characteristics when said switchable connections are individually
5 activated.

1 6. (original) The crosspoint switch integrated circuit of claim 5 wherein at
2 least some of said switchable connections are arranged in electrical parallel
3 and said components include capacitors and resistors.

1 7. (original) The crosspoint switch integrated circuit of claim 5 wherein at
2 least some of said switchable connections are arranged in electrical parallel
3 and said components include an inductor and a resistor.

1 8. (original) The crosspoint switch integrated circuit of claim 5 wherein said
2 switches are transistors and said components include at least some of
3 resistors, capacitors, or inductors.

1 9. (original) The crosspoint switch integrated circuit of claim 4 wherein
2 adjustable equalizers are coupled to said input ports in one-to-one
3 correspondence.

1 10. (cancelled)

1 11. (cancelled)

1 12. (currently amended) A crosspoint switching arrangement comprising:
2 a plurality of input ports connected to channels having
3 non-uniform frequency responses with respect to incoming signal trans-
4 missions;
5 a plurality of output ports connected to channels having
6 non-uniform frequency responses with respect to outgoing signal trans-
7 missions;
8 a switch matrix enabled to dynamically reconfigure connections
9 of said input ports to said output ports; and
10 equalization circuitry coupled to one of said input and output
11 ports, said equalization circuitry including a separate equalization circuit
12 for each said channel for which equalization is to be applied, each said
13 equalization circuit having a plurality of available configurations of equaliza-
14 tion, wherein selection of one of said available configurations for a particular
15 equalization circuit establishes circuits having filtering characteristics that are
16 tailored on a basis of said frequency responses of said channels to which said
17 specific ones of said input and output ports are [connected.] connected, each
18 said equalization circuit being dedicated to a particular said channel;
19 wherein said crosspoint switching arrangement is an integrated
20 circuit having said input ports, said output ports, said switch matrix and said
21 equalization circuitry.

1 13. (cancelled)

1 14. (currently amended) The crosspoint switching arrangement of claim 12
2 further comprising memory configured to store equalization settings for said
3 equalization circuitry, ~~said equalization circuitry including a separate~~
4 ~~equalization circuit for each said channel for which equalization is to be~~
5 ~~applied, each said equalization circuit having adjustable said filtering~~
6 ~~characteristics within a fixed number of available configurations, said~~
7 equalization settings stored at said memory including a selection of a
8 particular available said configuration for each said equalization circuit.

1 15. (original) The crosspoint switching arrangement of claim 14 wherein
2 each said equalization circuit includes a default configuration of first
3 connected circuit components and a plurality of alternative configurations,
4 said default configuration achieving a first level of frequency-dependent
5 compensation for effects of skin loss in signals conducted via said channels.

1 16. (original) The crosspoint switching arrangement of claim 15 wherein
2 each said alternative configuration introduces second connected circuit
3 components to achieve different levels of frequency-dependent compensation
4 for said effects of skin loss.

1 17. (original) The crosspoint switching arrangement of claim 16 wherein said
2 second connected circuit components are coupled to switches that selectively
3 introduce said second connected circuit components, said switches being
4 manipulated based upon said equalization settings stored in said memory.

1 18. (original) The crosspoint switching arrangement of claim 17 wherein said
2 equalization circuits are coupled to said input ports and are individually
3 adjustable from an exterior of an integrated circuit chip package in which said
4 equalization circuits and switch matrix reside.

1 19. (currently amended) A method of providing equalization for a crosspoint
2 formed on an integrated circuit chip switch comprising:
3 determining signal characteristics related to signal transmissions
4 via each of a plurality of ports of said crosspoint switch, including providing
5 on-chip measurements of jitter of electrical signals, wherein said jitter is
6 induced by off-chip conditions; and
7 setting equalization circuitry housed within said crosspoint
8 switch such that each said port has filtering characteristics tailored on a
9 basis of said signal characteristics for said signal transmissions via said
10 each port, said setting being automated and being at least partially based on
11 said on-chip measurements of jitter.

1 20. (currently amended) The method of claim 19 wherein said step of setting
2 includes selectively activating and deactivating switching devices which
3 introduce parallel connections of resistances and capacitances within said
4 adjustable equalization circuitry, said equalization circuitry being a plurality of
5 adjustable equalization circuits.

1 21. (currently amended) The method of claim 19 wherein said step of setting
2 includes selectively activating and deactivating switching devices which
3 introduce series connections of resistances and inductances within said
4 adjustable equalization circuits.

1 22. (original) The method of claim 19 wherein said step of setting includes
2 activating adaptive equalization circuitry.

1 23. (cancelled)

1 24. (cancelled)

1 25. (new) The crosspoint switch integrated circuit of claim 1 wherein said
2 equalization circuitry includes a multiplexer connected to a jitter measurement
3 component for providing said jitter measurements, said multiplexer being
4 connected to receive said electrical signals from each of said input ports and
5 being operatively associated with said jitter measurement component to
6 enable said jitter measurements on a port-by-port basis.

1 26. (new) The crosspoint switch integrated circuit of claim 25 wherein said
2 jitter measurement component includes a phase-locked loop for tracking data
3 transactions within said electrical signals, said jitter measurement component
4 further including a voltage-controlled oscillator connected to be responsive to
5 operations of said phase-locked loop.

1 27. (new) The crosspoint switch integrated circuit of claim 1 wherein said
2 equalization circuitry is configured to recurrently execute said jitter
3 measurements and recurrently execute responsive selection of said levels of
4 equalization for individual said input ports, thereby enabling said levels of
5 equalization to track variations in said transmission losses.